Polmaddie3 User Manual

Issue – 1.0

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Foreword

PLEASE READ THIS ENTIRE MANUAL BEFORE PLUGGING IN OR POWERING UP YOUR POLMADDIE3 BOARD.
PLEASE TAKE SPECIAL NOTE OF THE WARNINGS WITHIN THIS MANUAL.

Trademarks

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Introduction

Welcome to your Polmaddie3 board. Polmaddie is Enterpoint's low cost product range that offers an economical way to begin programming with CPLDs and FPGAs.

The aim of this manual is to assist in using the main features of Polmaddie3.

The Polmaddie board comes in several variants based on different devices. Polmaddie3 is based on a Xilinx™ Spartan3-50AN-4TQG144C .

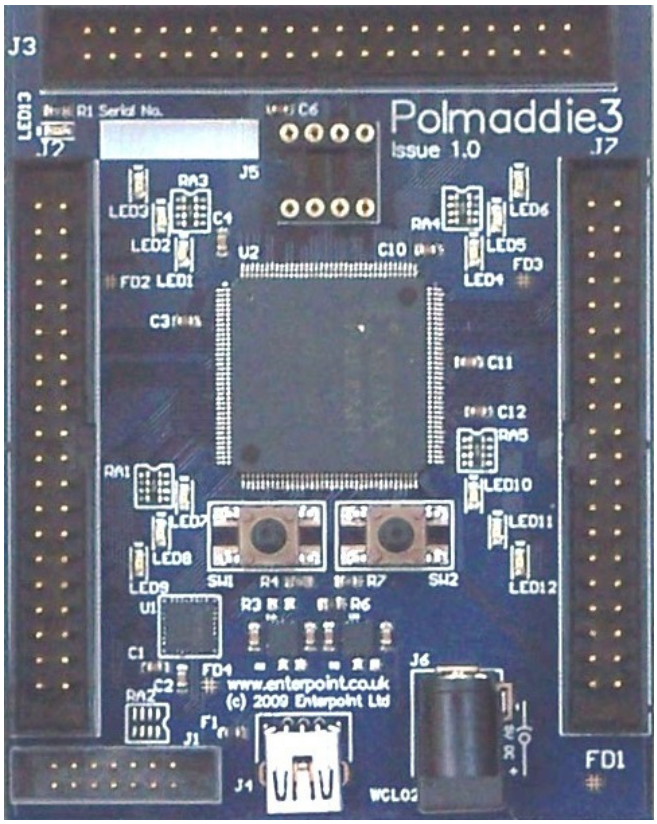

Figure 1 – Polmaddie3 Board

Finding Your Way Around

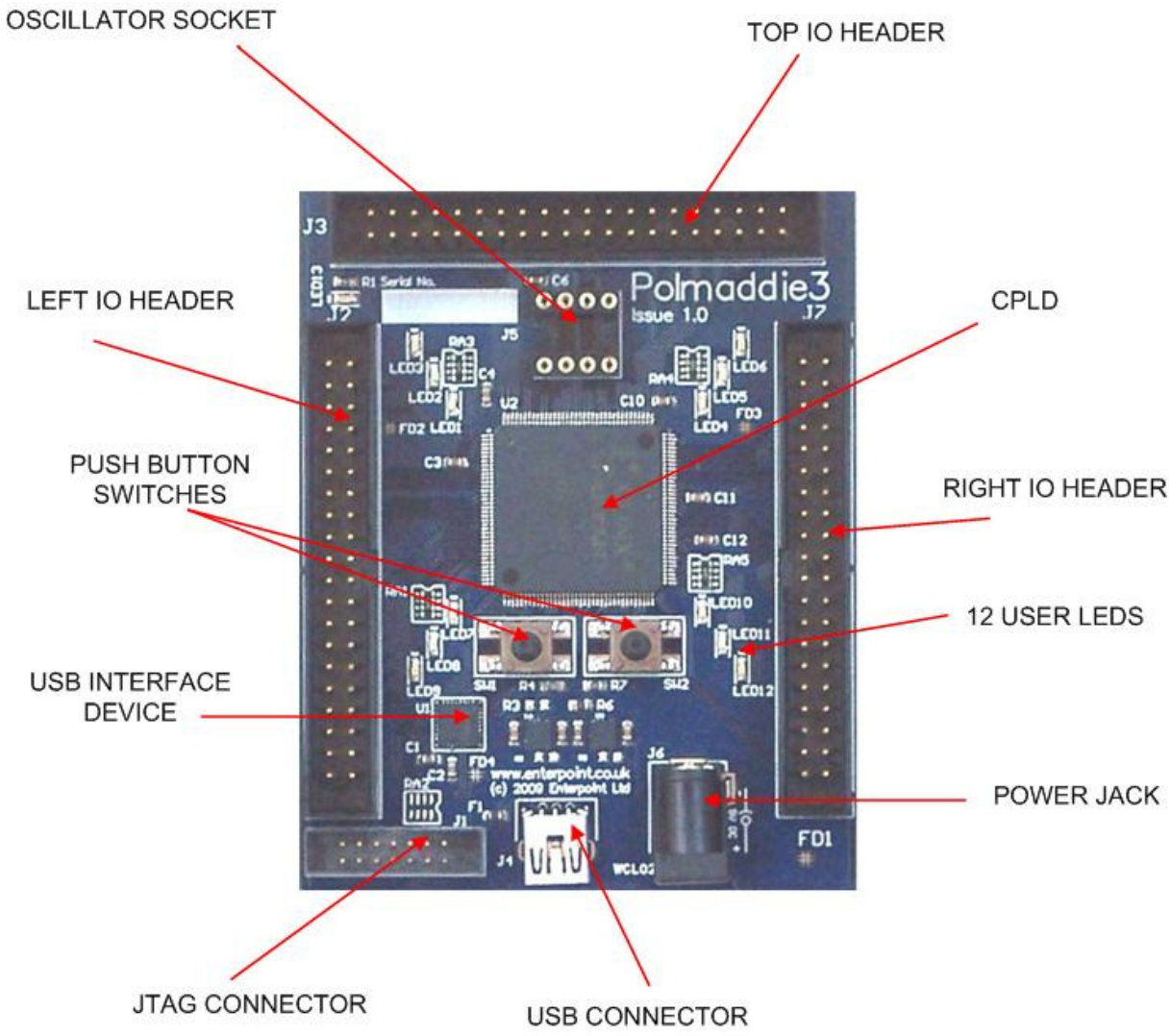

Figure 2 – Polmaddie3 Features.

Getting Started

Your Polmaddie3 will be supplied pre-programmed with a 'traffic lights' test design. The test design will allow the user to determine that the LEDs and the push button switches of the Polmaddie3 board are working. To use this test you must do the following:

(1) Apply power to the Polmaddie3 board, either by connecting a 5V power supply to the 2.1mm jack socket or by plugging a cable into the USB socket, either from a USB power supply adapter or a PC. The current consumed by the Polmaddie3 running the test program is approximately 60mA.

(2) The LEDs should light in a 'traffic lights' sequence. There is also a green Power indicator LED which will light to show that power is present and the 3.3V regulator is working.

(3) Press SW1 (This is the left Push Button switch). The traffic lights sequence will pause while the switch is activated and continue when the switch is released.

(4) Press SW2 (This is the right Push Button switch). The traffic lights sequence will pause while the button is activated and restart from the beginning of the sequence when the switch is released.

Polmaddie3 Features

Power Input

Polmaddie3 is powered either by connecting a 5V power supply to the 2.1mm jack socket or by plugging a cable into the USB socket, either from a USB power supply adapter or a PC.

The 5V supply is used to power the USB interface and to supply two regulators, one producing 1.2V for the FPGA core and the other producing 3.3V to power the FPGA IOs, the LEDs and the oscillator. 3.3V is also available on pin 2 of each of the IO headers. If you decide to use this as a source of power for external circuitry please remember that the maximum total power available from the 3.3V Regulator is 1 Amp.

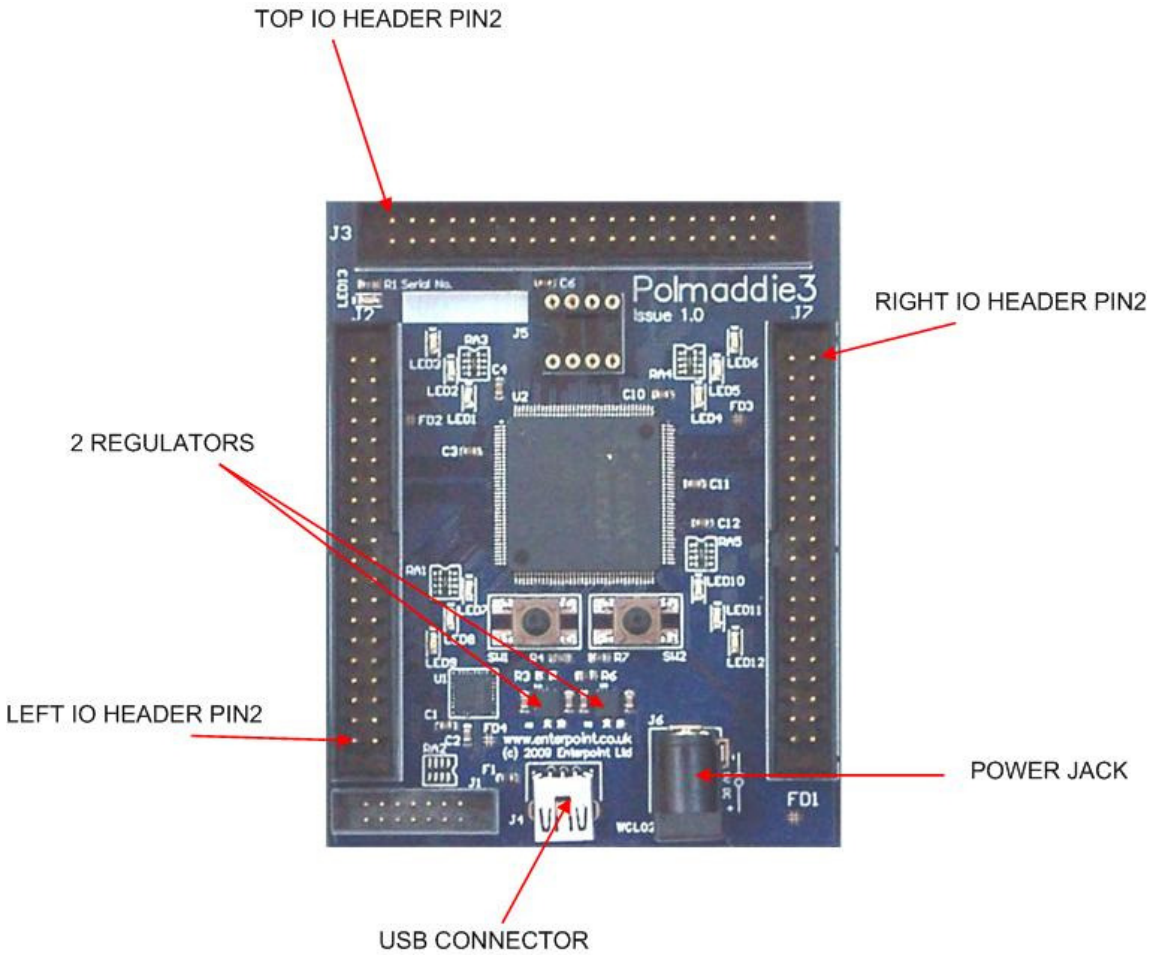

Figure 3 – Polmaddie3 Power Supply Features.

ARNING – THE REGULATORS MAY BECOME HOT IN NORMAL OPERATION ALONG WITH THE BOARDS THERMAL RELIEF. PLEASE DO NOT TOUCH OR PLACE HIGHLY FLAMABLE MATERIALS NEAR THESE DEVICES WHILST THE POLMADDIE1 BOARD IS IN OPERATION.

IO Headers

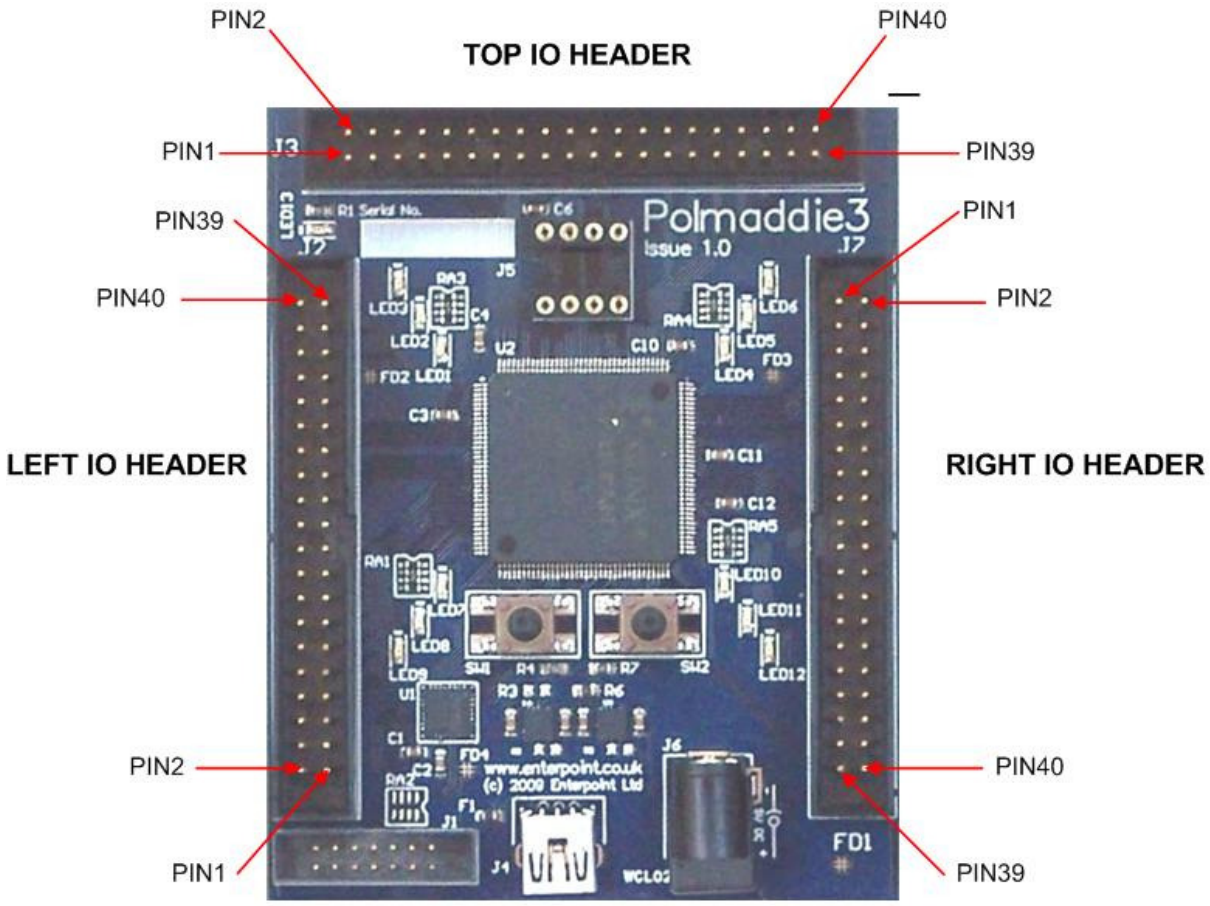

Figure 4 – Polmaddie3 Headers

The three 40-pin IDC Headers provide a simple mechanical and electrical interface for external signal inputs. The connectors on this header are on a 0.1inch (2.54mm), pitch and allow other electronic circuitry or user-designed add-on boards to be connected.

The headers each have 20 IOs routed to the CPLD. These are NOT 5V tolerant, the maximum input voltage should be limited to 3.3V. They each also have a permanent positive power pin on pin 2 and 19 permanent 0V connections as shown below:

LEFT HEADER					TOP HEADER					RIGHT HEADER				
PIN	USE	FPGA PIN	PIN	USE	PIN	USE	FPGA PIN	PIN	USE	PIN	USE	FPGA PIN	PIN	USE
1	IO40	30	2	3.3V	1	IO20	142	2		1	IO60	105	2	3.3V
3	IO39	29	4	0V	3	IO19	141	4	0V	3	IO59	104	4	0V
5	IO38	28	6	0V	5	IO18	139	6	0V	5	IO58	103	6	0V
7	IO37	27	8	0V	7	IO17	138	8	0V	7	IO57	102	8	0V
9	IO36	25	10	0V	9	IO16	135	10	0V	9	IO56	101	10	0V
11	IO35	24	12	0V	11	IO15	134	12	0V	11	IO55	99	12	0V
13	IO34	21	14	0V	13	IO14	132	14	0V	13	IO54	98	14	0V
15	IO33	20	16	0V	15	IO13	131	16	0V	15	IO53	96	16	0V
17	IO32	19	18	0V	17	IO12	130	18	0V	17	IO52	93	18	0V
19	IO31	18	20	0V	19	IO11	129	20	0V	19	IO51	92	20	0V
21	IO30	16	22	0V	21	IO10	127	22	0V	21	IO50	91	22	0V
23	IO29	15	24	0V	23	IO9	126	24	0V	23	IO49	90	24	0V
25	IO28	13	26	0V	25	IO8	125	26	0V	25	IO48	88	26	0V
27	IO27	12	28	0V	27	IO7	121	28	0V	27	IO47	87	28	0V
29	IO26	11	30	0V	29	IO6	120	30	0V	29	IO46	86	30	0V
31	IO25	10	32	0V	31	IO5	117	32	0V	31	IO45	84	32	0V
33	IO24	8	34	0V	33	IO4	116	34	0V	33	IO44	83	34	0V
35	IO23	7	36	0V	35	IO3	115	36	0V	35	IO43	82	36	0V
37	IO22	6	38	0V	37	IO2	114	38	0V	37	IO42	76	38	0V
39	IO21	5	40	0V	39	IO1	113	40	0V	39	IO41	75	40	0V

FPGA

The main device on the Polmaddie3 is the Xilinx™ Spartan3 XC3S50AN-4TQG144C, which has 50,000 gates and 1Mbit internal flash memory for configuration.

OSCILLATOR

The single oscillator socket on Polmaddie3 supports a 3.3V, 8-pin DIL outline oscillator. This clock signal is routed directly through to the CPLD on **pin 124**, which is a global clock input.

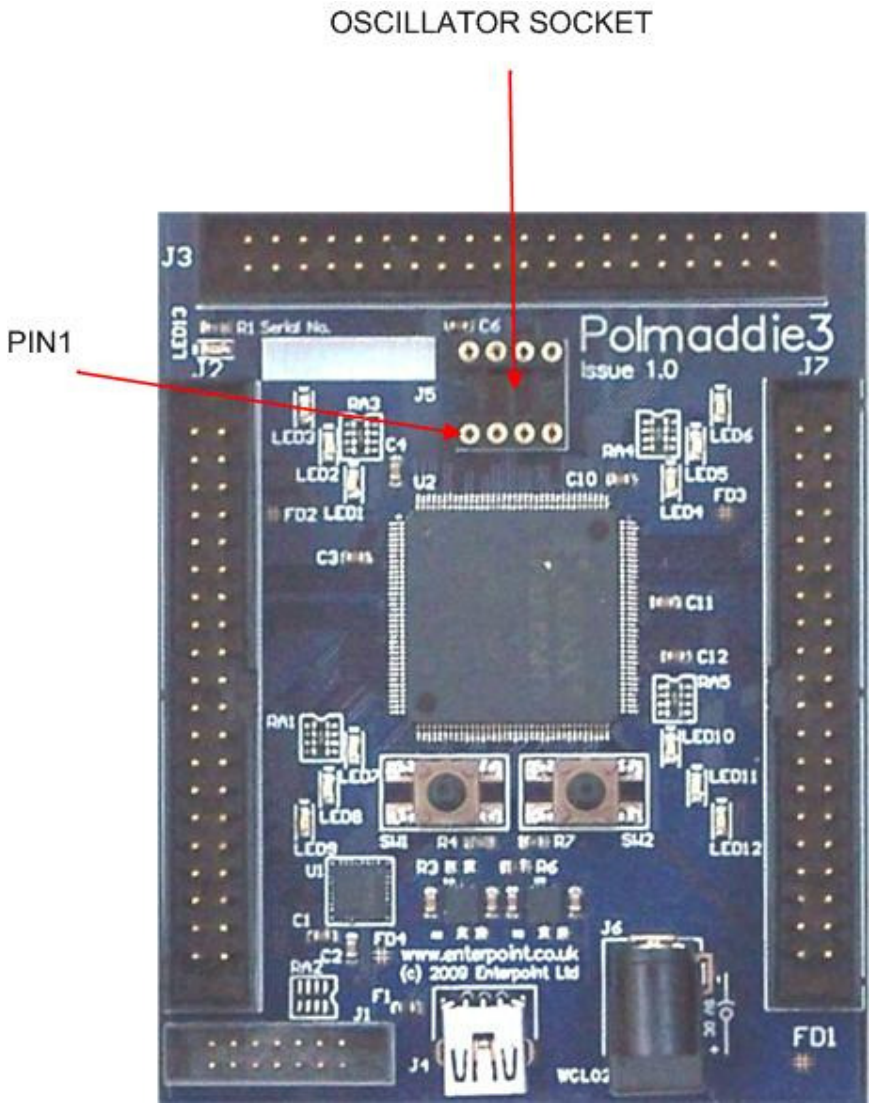

Figure 5 – Polmaddie3 Oscillator

LEDs

Polmaddie3 has 13 LEDS.

LED 13 is a green power indicator LED and indicates the presence of the 3.3V supply. It cannot be controlled by the CPLD.

LEDs 1 to 12 are arranged in 4 blocks of three, each block having one red, one orange and one green LED. This means they can be used to simulate traffic lights. They are all controlled by the CPLD. They connect to the CPLD as shown below:

LED	FPGA PIN	COLOUR	LED	FPGA PIN	COLOUR
LED1	4	GREEN	LED7	42	GREEN
LED2	3	ORANGE	LED8	32	ORANGE
LED3	58	RED	LED9	31	RED
LED4	110	GREEN	LED10	77	GREEN
LED5	111	ORANGE	LED11	78	ORANGE
LED6	112	RED	LED12	79	RED

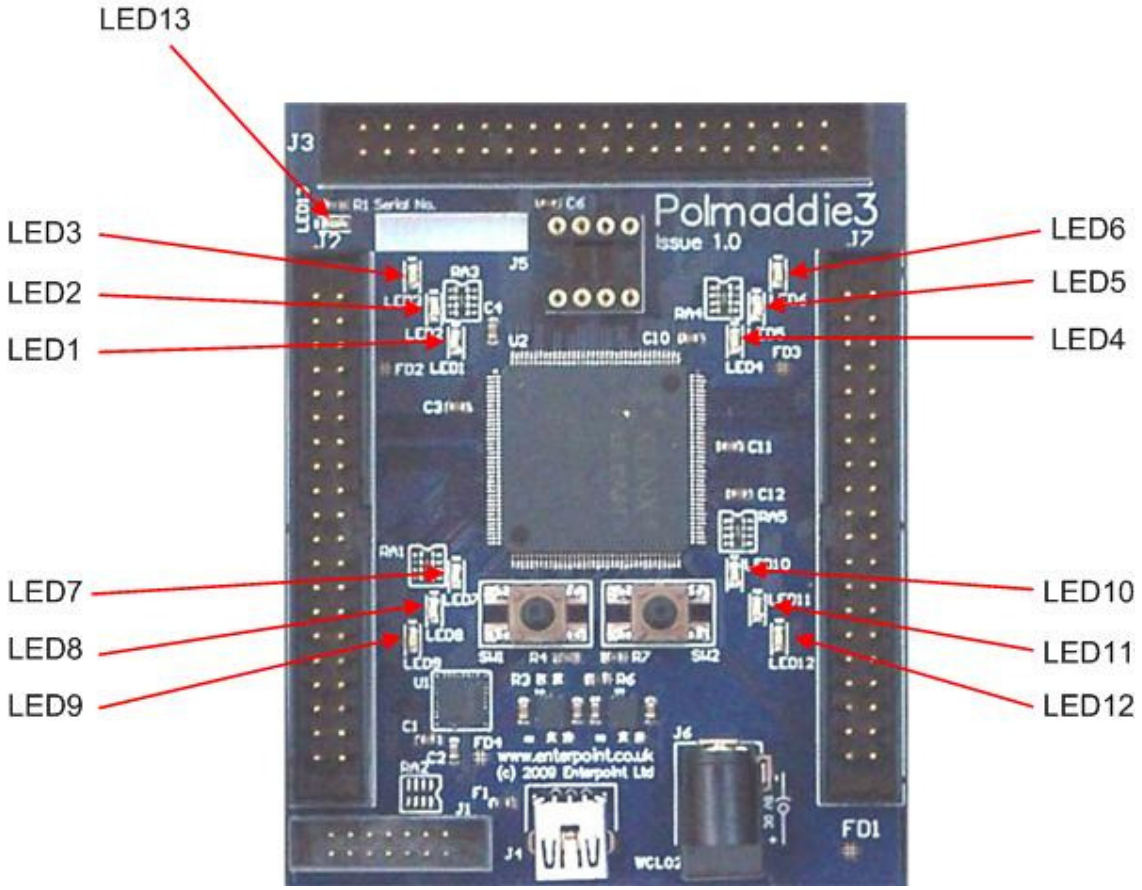

Figure 6 – Polmaddie3 LEDs

Switches

Polmaddie3 has two push button switches; to use these switches the IO pins connected to the switches must have a pull up resistor setting in the constraints file. This means that when a switch is activated a low level signal will be detected on the FPGA pin.

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The two switches are connected to the following IO pins:

SWITCH 1	SWITCH 2
49	70

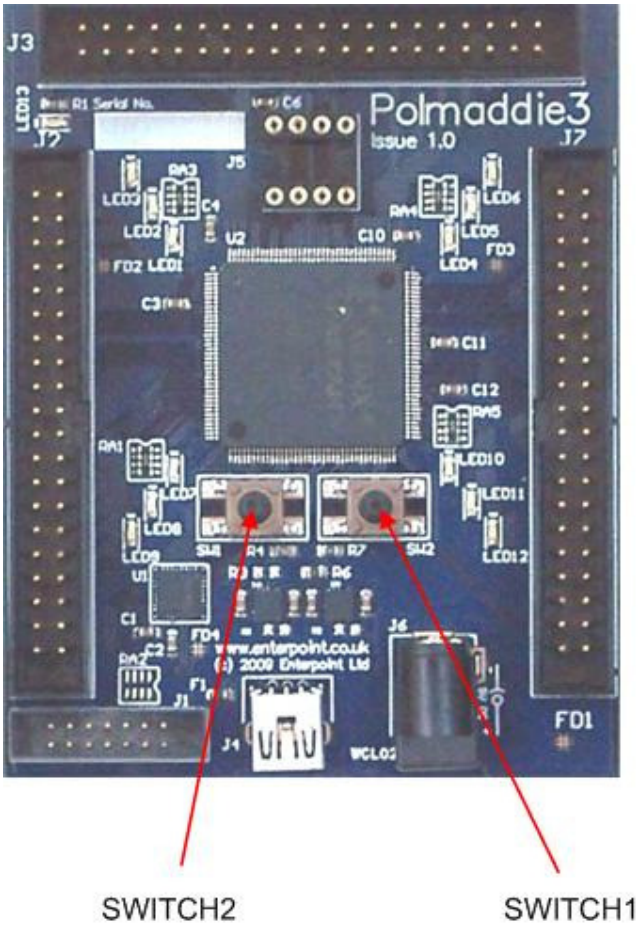


Figure 7– Polmaddie3 Switches

USB Interface

The USB interface on the Polmaddie3 is achieved using an FT232R USB to serial UART interface. The datasheet and drivers for this device are available from http://www.ftdichip.com. When appropriate drivers are installed the Polmaddie3 USB port should be detected as a serial port. Alternative data optimised drivers are also available from FTDI.

The FT232R is connected to the FPGA and provided a simple UART, or other converter, is implemented then the data sent over the USB serial port can be used either as control and/or data information. This allows a host computer to act in a number of ways including system control and data storage functions.

The FT232R can also supply a clock to the FPGA using CBUS4 I/O. This I/O can be programmed by tools available from FTDI to output different frequencies or other functions. The FT232R can provide clock frequencies of 6/12/24/48MHz.

The connections between the USB device and the FPGA are shown below:

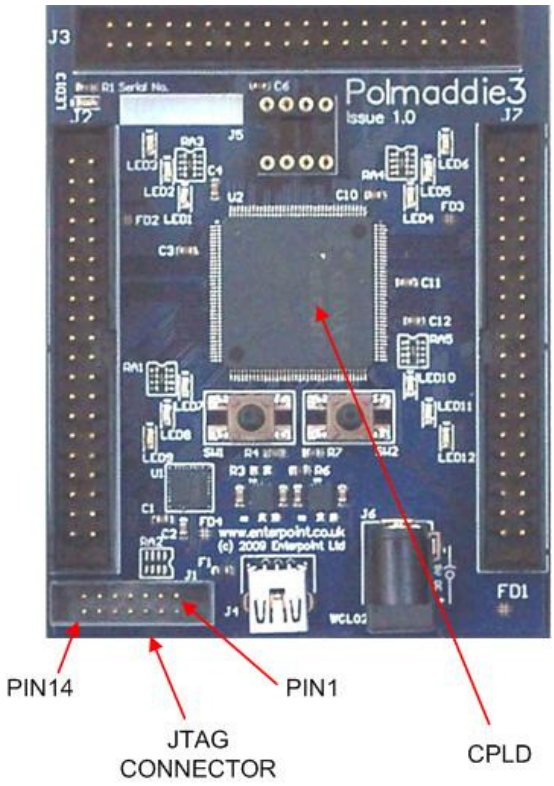
FT232R	FPGA PIN
CBUS4 (USB CLOCK)	54
CTS#	46
DCD#	47
DSR#	48
RI#	55
RTS#	60
DTR#	68
TXD	69
RXD	57

The FT232R connections CBUS0 to CBUS3 are routed via a resistor array site RA2 (resistor array not fitted) to the JTAG connector for future use in reconfiguring the FPGA via a USB interface, a scenario which is theoretically possible but not so far established. These connections, were the resistor array to be fitted, would be as shown below:

FT232R	JTAG SIGNAL
CBUS0	TMS
CBUS1	TCK
CBUS2	TDI
CBUS3	TDO

Programming Polmaddie3

The programming of the CPLD on Polmaddie3 can be achieved using the XILINX ISE tool iMPACT. It is anticipated that a JTAG connection will be used in conjunction with this software. There is a single JTAG chain on Polmaddie3 which allows the programming of the FPGA.



The JTAG connector has a layout as follows:

GND	GND	GND	GND	GND	GND	GND (pin1)
NC (pin14)	NC	TDI	TDO	TCK	TMS	3V3

Using the Xilinx iMPACT software the JTAG chain appears like this:

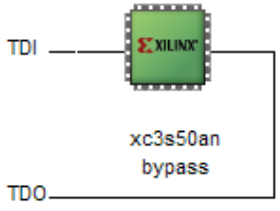


Figure 9 – Polmaddie3 JTAG CHAIN

Generation of suitable .bit files and control of the JTAG chain can be achieved using the XILINX ISE tool IMPACT. The .bit file can be used to program the FPGA only or the FPGA and its internal flash memory.

Mechanical Arrangement

Dimensions are in millimetres. The three 40-way connectors are arranged on a 0.1 inch grid relative to eachother.

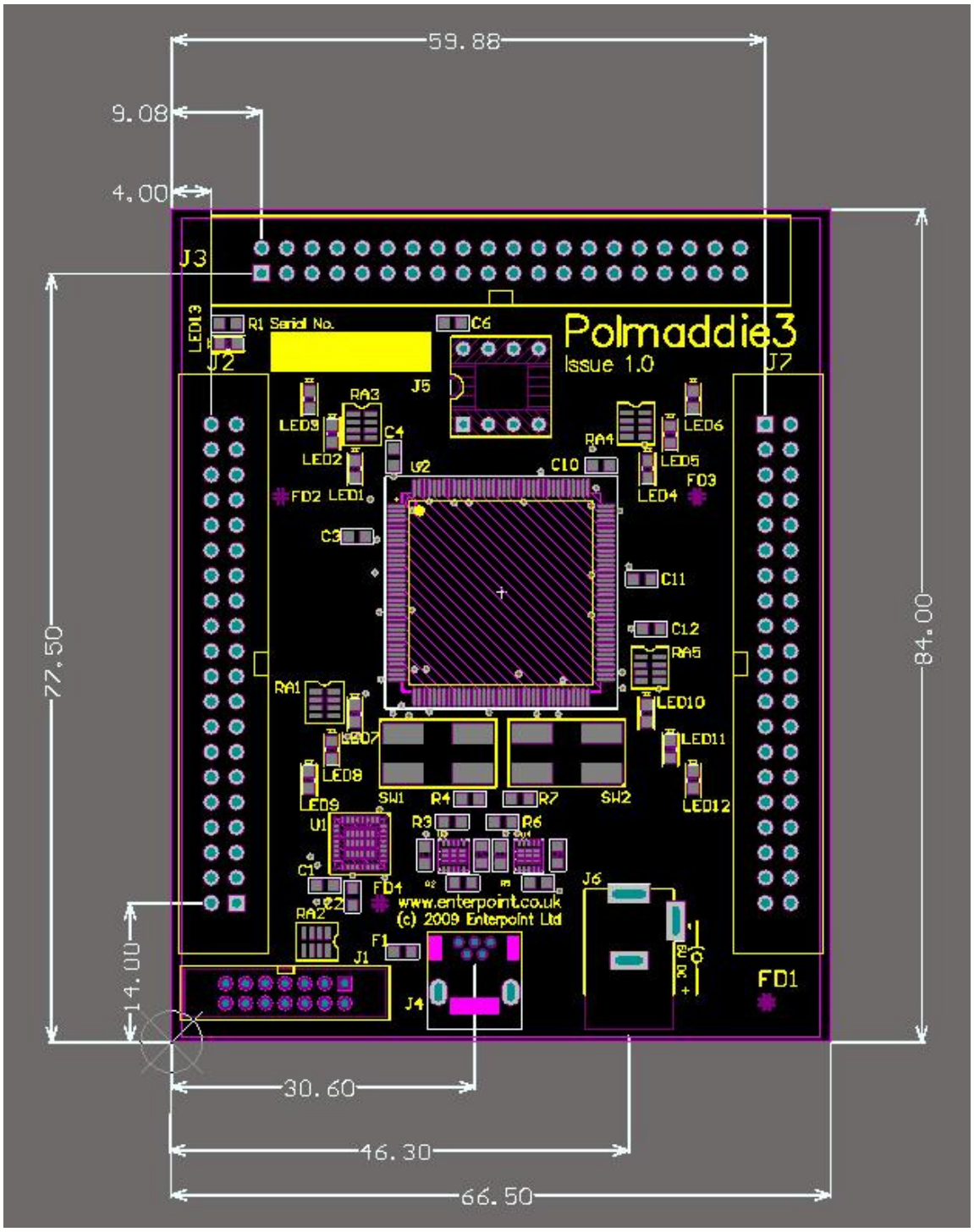


Figure 10– Polmaddie3 Mechanical Arrangement

Medical and Safety Critical Use

Polmaddie3 boards are not authorised for the use in, or use in the design of, medical or other safety critical systems without the express written person of the Board of Enterpoint. If such use is allowed the said use will be entirely the responsibility of the user. Enterpoint Ltd will accepts no liability for any failure or defect of the Polmaddie3 board, or its design, when it is used in any medical or safety critical application

Warranty

Polmaddie3 comes with a 90 return to base warranty. Enterpoint reserves the right not honour a warranty if the failure is due to maltreatment of the Polmaddie3 board.

Outside the warranty period Enterpoint offers a fixed price repair or replacement service. We reserve the right not to offer this service where a Polmaddie3 has been maltreated or otherwise deliberately damaged. Please contact support if need to use this service.

Other specialised warranty programs can be offered to users of multiple Enterpoint products. Please contact sales on boardsales@enterpoint.co.uk if you are interested in these types of warranty,

Support

Enterpoint offers support during normal United Kingdom working hours 9.00am to 5.00pm. Please examine our Polmaddie3 FAQ web page and the contents of this manual before raising a support query. We can be contacted as follows:

Telephone - +44 (0) 121 288 3945
Email - support@enterpoint.co.uk